Read the README.blif file first

The implementation of the machine control system had required five states, two of them are for the starting point of the machine and other three for each section.

When turned on the machine require three consecutive bit T taken to the FSM, which will respond with the correct gates opening. The data path analyzes gates to open the correct registers. On overflow error registers will reset. from the second cycle and on, the first state will require only one T bit to proceed (the 5th state).

The system is divided into FSM (finite state machine) and DP (Data path).

The FSM acquires the signals to shut down the machine on errors, and the first three inputs bits; it takes care of switching the machines on and off and what decide what to do with inputs and gates.

The DP takes the current state throw opened gate. It takes directly load bits and arrange counters.

Following a flow chart of each file with relative variables between them.

print\_stats before

FSMD pi= 7 po=30 nodes=234 latches=37

lits(sop)= 517

sis> print\_stats after

FSMD pi= 7 po=30 nodes=205 latches=37

lits(sop)= 439